(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 006 527 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
07.06.2000 Bulletin 2000/23

(51) Int. Cl.[7]: G11B 20/10, H03M 13/41, G11B 20/14

(21) Application number: 99309596.7

(22) Date of filing: 30.11.1999

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 04.12.1998 JP 36189998
02.06.1999 JP 15567399

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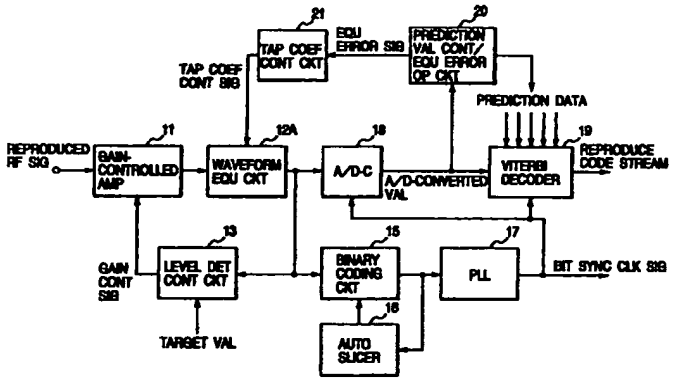
(54) A decoding apparatus

(57) An waveform equalizer equalizes the signal reproduced from an optical disc to remove reproduction waveform distortion with a frequency characteristic controlled. A binary coder and a PLL circuit generate a bit clock. An a/d converter a/d-converts the equalized signal in response to the bit clock. A Viterbi decoder including metric operation decodes the output of the a/d converter in response to the bit clock. The metric operation generates a metric operation result from an output of the a/d-converter and prediction data. The Viterbi decoder decodes the output of the a/d converter through the metric operation according to prediction data. An operating circuit generates an equalizing error from the output of a/d converter and a waveform equalizing target. A coefficient generator controls the frequency characteristic according to the equalizing error to minimize the equalizing error. The prediction data for the metric operation is obtained from the output of the a/d converter for better decoding.

FIG. 1



EP 1 006 527 A1

Description

[0001] This invention relates to a decoding apparatus, particularly to a decoding apparatus for decoding a signal reproduced from an optical disc.

[0002] A decoding apparatus for decoding a signal reproduced from an optical disc is known.

[0003] Fig. 11 is a block diagram of a prior art decoding apparatus for decoding a signal reproduced from an optical disc. In Fig. 11, an RF (radio wave frequency) signal reproduced from an optical disc is supplied a gain-controlled amplifier 11. The gain-controlled amplifier 11 amplifies the RF signal with its envelope level kept constant in accordance with a gain control signal. An output of the gain-controlled amplifier 11 is supplied to a waveform equalizing circuit 12. The waveform equalizing circuit 12 removes a waveform distortion caused by lack of transmission bandwidth, that is, waveform-shapes the output of the gain-controlled amplifier 11. A level detection and controlling circuit 13 compares an envelope level of an output of the waveform equalizing circuit 12 with a target value and generates a gain control signal to make the envelop level equal to the target value to control the gain of the gain controlled amplifier 11.

[0004] An output of the waveform equalizing circuit 12 is supplied to one input of an adder 14. A binary coding circuit 15 binary-codes the output of the adder 14 such that the output of the adder 14 compared with a center level to output a reproduced code stream. The reproduced code stream is also supplied to a PLL (Phase Locked Loop) circuit 17 and to an automatic slicer 16.

[0005] The automatic slicer 16 generates a level adjusting signal from the reproduced code stream and supplies it to another input of the adder 14 to adjust the center level of the output of adder to prevent binary-coding error caused by asymmetric waveforms which may be generated in accordance with a molding condition of the optical disc. The PLL circuit 17 generates a bit synchronizing clock from the reproduced code stream.

[0006] In this prior art decoding apparatus, the binary coding circuit only binary-codes the output of the adder 14 by comparing the output of the adder 14 with a center line level adjusted, so that if skew occurs in a relative angle between the optical pickup generating the RF signal and the optical disc, there is a tendency that the S/N ratio becomes insufficient.

[0007] Moreover, another prior art decoding apparatus including Viterbi decoder is known. Fig. 12 is a block diagram of such a prior art Viterbi decoder described in "PIONEER R&D" (Vol. 6. No. 2). In Fig. 12, a reproduced signal from an optical head is supplied to an a/d converter 101. An output of the a/d converter 101 supplied to a Viterbi decoder. The Viterbi decoder includes a branch metric operation circuit 102 for effecting a branch metric operation with the output of the a/d converter 101 and first to third prediction values to output a square error between the reproduced sample value and the first to third prediction values, a path metric operation circuit 103 for effecting a path metric operation, and a path memory 104 for storing an output of the path metric operation circuit 103.

[0008] The output of the Viterbi decoder is supplied to an eight/sixteen demodulator 105.

[0009] The a/d converter 101 a/d-converts the reproduced signal and limits peak values. The Viterbi decoder effects Viterbi decoding processing including the metric operation with only three fixed values of prediction data, that is high, zero, and low values to output a reproduced code stream.

[0010] In this prior art decoding apparatus, there is a problem in that the metric characteristic which the reproduced signal inherently has is insufficiently used.

[0011] The aim of the present invention is to provide an improved decoding apparatus.

[0012] According to the present invention, a first decoding apparatus for decoding a signal reproduced from an optical disc is provided which includes: a gain control circuit for controlling an envelope level of a waveform of the signal to a predetermined level; an waveform equalizing circuit having a frequency characteristic for waveform-equalizing the signal from the gain control circuit to remove reproduction waveform distortion of the signal, the frequency characteristic being changed in accordance with at least a tap coefficient; a binary coding circuit for binary-coding an output of the waveform equalizing circuit; a phase-locked-loop circuit for generating a bit synchronizing clock signal on the basis of an output of the binary coding circuit; an a/d converting circuit for a/d-converting an output of the waveform equalizing circuit in response to the bit synchronizing clock signal; a Viterbi decoding circuit including a metric operation circuit for Viterbi-decoding the output of the a/d converting circuit in response to the bit synchronizing clock signal to output a bit stream, the metric operation circuit generating a metric operation result from an output of the a/d-converting circuit and prediction data, the Viterbi decoding circuit Viterbi-decoding the output of the a/d converting circuit with the metric operation result; an operating circuit for operating an equalizing error from the output of a/d converting circuit and a waveform equalizing target value; a coefficient generation circuit for generating the tap coefficient from the equalizing error to minimize the equalizing error; and a circuit for operating the prediction data from the output of the a/d converting circuit.

[0013] According to the present invention, a second decoding apparatus for decoding a signal reproduced from an optical disc is provided which includes: an automatic gain control circuit for controlling an envelope level of a waveform of the signal to a predetermined level; a waveform equalizing circuit having a frequency characteristic for waveform-equalizing the signal from the automatic gain control circuit to remove reproduction waveform distortion of the signal, the frequency

characteristic being changed in accordance with at least a tap coefficient; an a/d converting circuit for a/d-converting an output of the waveform equalizing circuit in response to a sampling clock signal; a bit clock operation and data estimating circuit responsive to said sampling clock signal for operating a bit synchronizing clock position from an output of the a/d converting circuit to generate a bit synchronizing clock signal and estimating a level of an output of the a/d converting circuit at the bit synchronizing clock position to output estimated data; a Viterbi decoding circuit including metric operation circuit for Viterbi-decoding the output of the a/d converting circuit in response to the bit synchronizing clock signal to output a bit stream, the metric operation circuit generating a metric operation result from an output of the a/d-converting circuit and prediction data, the Viterbi decoding circuit Viterbi-decoding the output of the a/d converting circuit with the metric operation result; an operating circuit for operating an equalizing error from the output of the a/d converting circuit and a waveform equalizing target value; a coefficient generation circuit for generating the tap coefficient from the equalizing error to minimize the equalizing error; and a circuit for operating the prediction data from the output of the a/d converting circuit.

[0014] The features of the present invention will become more readily apparent from the following detailed description of exemplary embodiments and the accompanying drawings, in which:

Fig. 1 is a block diagram of a decoding apparatus according to a first embodiment of this invention;
Fig. 2 is a block diagram of the waveform equalizing circuit shown in Fig. 1;
Fig. 3A is a graphical drawing of a prior art showing an eye pattern of a waveform equalizing circuit without adaptive waveform equalizing;
Fig. 3B is a graphical drawing of the first embodiment showing an eye pattern observed at the waveform equalizing circuit shown in Fig. 1;
Fig. 4 is a graphical drawing of the first embodiment showing target values of waveform equalizing;
Fig. 5A is an illustration of this embodiment showing condition transition of the Viterbi decoder shown in Fig. 1;
Fig. 5B is a table of this embodiment showing a relation between the condition transition shown in Fig. 5A and data;
Fig. 6 is an illustration of the first embodiment showing a trellis diagram of the Viterbi decoder shown in Fig. 1;
Fig. 7 is a graphical drawing of the first embodiment showing a histogram of a/d coding results;
Fig. 8 is a graphical drawing of the first embodiment showing a relation between the signal to noise ratio and the error rate according to this embodiment;
Fig. 9 is a block diagram of a decoding circuit of a second embodiment;
Figs. 10A to 10E are time charts of the second embodiment illustrating the operation of the data estimating PLL circuit shown in Fig. 9;
Fig. 11 is a block diagram of a prior art decoding apparatus for decoding a signal reproduced from an optical disc;
Fig. 12 is a block diagram of a prior art Viterbi decoder;
Fig. 13 is a block diagram of the prediction data controlling and equalizing error operation circuit shown in Figs. 1 and 9; and
Fig. 14 is a block diagram of the data estimating PLL circuit according to the second embodiment.

[0015] The same or corresponding elements or parts are designated with like references throughout the drawings.

〈FIRST EMBODIMENT〉

[0016] Fig. 1 is a block diagram of a decoding apparatus according to a first embodiment of this invention.

[0017] An RF (radio wave frequency) signal reproduced from an optical disc is supplied to a gain-controlled amplifier 11. The gain-controlled amplifier 11 amplifies the RF signal with envelope level kept constant in accordance with a gain control signal. An output of the gain-controlled amplifier 11 is supplied to a waveform equalizing circuit 12A. The waveform equalizing circuit 12A removes a waveform distortion caused by lack of transmission bandwidth, that is, the waveform equalizing circuit 12A waveform-shapes the output of the gain-controlled amplifier 11 with its frequency characteristic controlled. An output of the waveform equalizing circuit 12A is supplied to a level detection and controlling circuit 13, an a/d converter 18, and a binary coding circuit 15. The level detection and controlling circuit 13 compares an envelope level of an output of the waveform equalizing circuit 12A with a target value and generates the gain control signal to make the envelop level equal to the target value to control the gain of the gain-controlled amplifier 11. The binary coding circuit 15 binary-codes the output of the waveform equalizing circuit 12A such that the output of the waveform equalizing circuit 12A is compared with a center level to output a reproduced code stream. The reproduced code stream is supplied to a PLL (Phase locked Loop) circuit 17 and to an automatic slicer 16.

[0018] The automatic slicer 16 generates a level adjusting signal from the reproduced code stream and supplies the level adjusting signal to the binary coding circuit 15 to adjust the center level for comparing to prevent binary-coding error caused by asymmetric waveforms which may be generated in accordance with a molding condition of the optical disc. The PLL circuit 17 generates a bit synchronizing signal from the reproduced code stream.

[0019] The a/d converter 18 a/d-converts the output

of the waveform equalizing circuit 12A in response to the bit synchronizing clock signal as a sampling pulse. An output of the a/d converter 18 is supplied to a Viterbi decoder 19 and a prediction data (values) controlling and equalizing error operation circuit 20 which obtains an equalizing error between equalizing target data and the output of the a/d converter 18. The equalizing error signal is supplied to a tap coefficient controlling circuit 21 which generates a tap coefficient control signal in accordance with the equalizing error signal. The tap coefficient control signal is supplied to the waveform equalizing circuit 12A to control the frequency characteristic of the waveform equalizing circuit 12A.

[0020] The prediction data controlling and equalizing error operation circuit 20 further generates prediction data (values) for metric operation of the Viterbi decoder 19 from the equalizing error signal.

[0021] The Viterbi decoder 19 decodes the output of the a/d converter 18 with the prediction data through the metric operation to output a reproduced code stream.

[0022] The operation will be described more specifically.

[0023] Fig. 2 is a block diagram of the waveform equalizing circuit 12A shown in Fig. 1. The waveform equalizing circuit 12A includes an input terminal 31 for inputting the output of the gain-controlled amplifier 11, tap coefficient control signal input terminals 32 to 34 for inputting tap coefficients C-1, C0, and C1, a delay 35 for delaying the output of the gain-controlled amplifier 11 by a predetermined interval, a delay 36 for delaying an output of the delay 35 by the predetermined interval, a multiplier M1 multiplies the output of the gain-controlled amplifier 11 by the tap coefficient C-1, a multiplier M2 multiplies the output of the delay 35 by the tap coefficient C0, a multiplier M3 multiplies the output of the delay 36 by the tap coefficient C1, and an adder 37 for adding the outputs of the multipliers M1, M2, and M3 to provide the output of the waveform equalizing circuit 12A. This structure controls the frequency characteristic of the waveform equalizing circuit 12A by controlling the tap coefficients C-1, C0, and C1 from the tap coefficient controlling circuit 21.

[0024] The prediction data controlling and equalizing error operation circuit 20 generates five prediction values (data) corresponding to converged levels of the sampled value of the a/d converter 18 on the basis of the output of the a/d converter 18 and operates the equalizing error in the waveform equalizing circuit 12A. The tap coefficient control circuit 21 adjusts the tap coefficients C-1, C0, and C1 such that the equalizing error is minimized or reduced.

[0025] In this embodiment, the number of the tap coefficients is three. However, this embodiment is applicable to a waveform equalizing supplied with more than three tap coefficients.

[0026] Fig. 13 is a block diagram of the prediction data controlling and equalizing error operation circuit 20 shown in Fig. 1.

[0027] The prediction data controlling and equalizing error operation circuit 20 includes a equalizing error operation circuit 51 for operating the equalizing error signal in accordance with the a/d-converted value and prediction target values and a prediction value control circuit 52 for generating mean values of the equalizing error in accordance with each prediction target value to supply the prediction data to the Viterbi decoder 19.

[0028] Fig. 3A is a graphical drawing of a prior art showing an eye pattern of a waveform equalizing circuit without adaptive waveform equalizing. Fig. 3B is a graphical drawing of this embodiment showing an eye pattern observed at the waveform equalizing circuit 12A with adaptive waveform equalizing. Fig. 4 is a graphical drawing of this embodiment showing target values of waveform equalizing. Fig. 5A is an illustration of this embodiment showing condition transition of the Viterbi decoder shown in Fig. 1. Fig. 5B is a table of this embodiment showing a relation between the condition transition shown in Fig. 5A and data. Fig. 6 is an illustration of the first embodiment showing a trellis diagram of the Viterbi decoder 19.

[0029] If waveform equalizing is effected without adaptive waveform equalizing, the eye pattern is observed as shown in Fig. 3A. On the other hand, if ideal waveform equalizing is effected by the waveform equalizing circuit 12A with adaptive waveform equalizing according to this embodiment, the eye patten is observed as shown in Fig. 3B. This waveform is provided with waveform equalizing with a partial response characteristic (1,1,1,1), that is, waveform equalizing to have response of 1,1,1, 1 at the bit synchronizing position in response to a single input pulse (isolated pulse). However, this embodiment is applicable to decoders using other partial response characteristics.

[0030] In Figs. 3A and 3B, arrows show sampling points. The a/d converter 18 a/d-converts the output of the waveform equalizing circuit 12A at the sampling points in response to the bit synchronizing clock signal, so that the a/d-converted values can be represented with either of five values which is nearest to the input of the a/d converter 18. The prediction data controlling and equalizing error operation circuit 20 operates the equalizing error from the equalizing target values and the a/d-converted signal and generates five prediction values (data) corresponding the five values for the a/d converting from the obtained equalizing error and supplies the five prediction values to the Viterbi decoder 19. The target values U, ML, 0, -MU, and -L for the waveform equalizing are set as shown in Fig. 4. Moreover, the prediction data controlling and equalizing error operation circuit 20 supplies the equalizing error signal to the tap coefficient controlling circuit 21.

[0031] The condition transition in the Viterbi decoder 19 is shown in Fig. 5A and the relation between the condition transition and the data is shown in Fig. 5B. A trellis diagram of the Viterbi decoder 19 is shown in

Fig. 6.

[0032] The equalizing error operation and the prediction value operation will be described more specifically.

[0033] The automatic gain control circuit including the gain-controlled amplifier 11 and the level detection and controlling circuit 13 keeps peak to peak values substantially constant. Therefore, if the symmetric characteristic and the waveform equalizing characteristic are ideal, the output of the a/d converter 18 converges on either of equalizing target values U, ML, 0, -MU, and -L.

[0034] The output of the a/d converter 18 is supplied to the prediction value controlling and equalizing error operation circuit 20 at every sampling to operate the equalizing error. It is assumed that the equation error at time k is ek. Then, ek is obtained from a difference between the sampled value and one of equalizing target values nearest to the sampled value. The tap coefficient control circuit 21 operates the tap coefficients C-1, Co, and C1 from the equalizing error ek at the time k. In this embodiment an example of operating by ZF (Zero-Forcing) algorithm is shown. That is, the tap coefficient operation in the tap coefficient control circuit 21 with the ZF algorithm is given by:

$$Cn[i+1] = Cn[i] - \alpha \times \Sigma \, sgn\,(S^{\wedge}(k-n) \times ek)$$

where Cn represents either of coefficients C-1, C0, and C1, i represents a coefficient renewing unit which is a predetermined interval defined by an operation clock signal, α is a renewing coefficient which is smaller than one, Σ represents a total of the number of samples at the renewing unit timing, and S^(k-n) represents an equation target value. That is, the $(i+1)^{th}$ tap coefficient indicates that the i^{th} tap is corrected with the second term of the above equation.

[0035] Moreover, the sgn function used in this equation is a signature function represented by:

$$sgn\,(x) = 1 \; (x > 0, x = 0)$$

$$sgn\,(x) = -1 \; (x < 0)$$

[0036] The tap coefficient control circuit 21 successively renews values of the tap coefficients C-1, C0, and C1 from the initial tap coefficient setting values in accordance with the equalizing error from the prediction value controlling and equalizing error operation circuit 20 with the above equation to supply the tap coefficient control signal to the waveform equalizing circuit 12A.

[0037] In this embodiment, the example of the operation according to the ZF algorithm. However, other known adaptive equalizing algorithms such as MSE (mean square error) algorithm are applicable.

[0038] Fig. 7 is a graphical drawing of this embodiment showing a histogram of a/d coding result.

[0039] When the signal to noise ratio is sufficient and symmetry of the reproduced signal is enough, there is a tendency that the sampled values converge on the equalizing target values U, MU, 0, -ML, and -L, so that it is sufficient that the equalizing target values can be used as the prediction values for the metric operation in the Viterbi decoder 19.

[0040] On the other hand, when the signal to noise ratio is insufficient and symmetry of the reproduced signal is not enough, it is insufficient that the equalizing target values are used as the prediction values for the metric operation in the Viterbi decoder 19 because a sufficient decoding characteristic cannot be obtained.

[0041] Fig. 7 shows such a condition. In this case, that is, when the symmetry is insufficient or waveform equalization is insufficiently effected, the prediction values for the metric operation is changed from the (prediction) target values U, MU, 0 -ML, and -L in accordance with the equalized waveforms (equalizing error) to improve the decoding characteristic of the Viterbi decoder 19.

[0042] The prediction data controlling and equalizing error operation circuit 20 generates the prediction values for the metric operation and supplies prediction values to the Viterbi decoder 19 as follows:

[0043] The prediction data controlling and equalizing error operation circuit 20 operates the equalizing error ek to a/d-converted values from the a/d converter 18 and obtains an average of the equalizing errors ek to the equalizing target values U, MU, 0, -ML, and -L. Moreover, the average of the equalizing error ek is obtained during obtaining the equalizing error and the prediction values are obtained by correcting the target values U, MU, 0, -ML, and -L.

[0044] The prediction data controlling and equalizing error operation circuit 20 and the tap coefficient control circuit 21 can be formed with discrete circuits such as multipliers and adders. However, it is also possible to form these circuits with microprocessors.

[0045] Fig. 8 is a graphical drawing of this embodiment showing a relation between the signal to noise ratio and the error rate according to this embodiment, wherein a prior art relation is also shown for reference.

[0046] In Fig. 8, the characteristic curve A shows the prior art relation between the signal to noise ration and the error rate and the characteristic curve B shows a relation between the signal to noise ratio and the error rate according to this embodiment using five prediction values for the Viterbi decoding. As clearly understood from the characteristic curve B in Fig. 8, the decoding apparatus of the first embodiment improves the error rate to the signal to noise ratio.

〈SECOND EMBODIMENT〉

[0047] Fig. 9 is a block diagram of a decoding circuit of a second embodiment. The decoding circuit of the second embodiment is substantially the same as that of the first embodiment. The difference is that the binary

coding circuit 15 and the automatic slicer 16 are omitted, the PLL circuit 17 is replaced with a data estimating PLL circuit 22 and the a/d-converter 18 is responsive to a sampling clock signal instead the bit synchronizing clock.

[0048] In this embodiment, the frequency of the sampling clock signal is slightly higher than that of the bit synchronizing signal. The a/d converter 18 converts the output of the waveform equalizing circuit 12A at the frequency sampling clock signal. The a/d converted signal is supplied to the data estimating PLL 22 which generates the bit synchronizing clock signals to supply it to the Viterbi decoder 19 and estimates the data at the timing of the bit synchronizing clock signal. The estimated data outputted from the data estimating PLL 22 is supplied to the prediction data controlling and equalizing error operation circuit 20 and the Viterbi decoder 19.

[0049] In this embodiment, the a/d-converting is performed after removing the waveform distortion by the waveform equalizing circuit 12A. However, it is also possible to a/d-convert the output of the gain-controlled amplifier 11 before the waveform equalizing circuit 12A.

[0050] Figs. 10A to 10E are time charts of the second embodiment illustrating the operation of the data estimating PLL circuit 22. The output of the waveform equalizing circuit 12A is a/d-converted at time k - 1, k, and k + 1 in response to the sampling clock signal as shown in Figs. 10A and 10C. A zero-cross point is detected between the data streams Xk-1 and Xk. This point provides a phase point which corresponds to a rising edge of a bit clock shown in Fig. 10A. Using this phase point, the data estimating PLL circuit 22 provides PLL operation with a loop filter and a VCO (not shown) in the data estimating/PLL circuit 22. This PLL operation and a logic operation (not shown) generates a second bit synchronizing clock as shown in Fig. 10D.

[0051] In response to the bit synchronizing clock signal, the data estimating PLL circuit 22 estimates the data at the rising edge of the bit synchronizing clock signal.

[0052] The data is estimated by the linear interpolating or the convolution operation from the sampled data. More specifically, in Fig. 10A, data S^n is obtained from data Xk-1 and data Xk and data S^n+1 is obtained from the data Xk and Xk+1 as shown in Fig. 10E.

[0053] With the estimated data from the data estimating PLL circuit 22 and the bit synchronizing clock, it is possible to generate the prediction values for the Viterbi decoder 19 and the tap coefficient signal for the waveform equalizing circuit 12A as similar to the first embodiment.

[0054] Moreover, if the a/d-converting is performed before the waveform equalizing circuit 12A, the similar operation is provided.

[0055] Fig. 14 is a block diagram of the data estimating PLL circuit 22 according to the second embodiment.

[0056] The data estimating PLL circuit 22 includes a sample interpolation circuit 61 for interpolating the sampled data Xk in response to the sampling clock signal, a reproduced bit synchronizing clock generator (phase detector) 62 for generating the reproduced bit synchronizing clock signal and a phase error signal, a digital loop filter 63 for filtering the phase error signal in response to the sampling clock signal, and a digital VCO 64 for generating the bit synchronizing phase signal in accordance with the filtered phase error signal in response to the sampling clock signal.

[0057] The data Xk sampled by the a/d converter 18 and the bit synchronizing phase signal (data point phase) are supplied to the sample interpolating circuit 61 which predicts the data value S^k from the data Xk and the data point phase by linear interpolation or the convolution operation.

[0058] The reproduced bit synchronizing clock generator 62 generates the reproduced bit synchronizing clock signal and the phase error signal from the data point phase (bit synchronizing phase signal) and the sampling clock signal. Because the frequency of the sampling clock signal has higher than that of the bit synchronizing clock signal, the reproduced bit synchronizing clock signal is generated such that pulses of the sampling clock signal are thinned.

[0059] The phase detection can be detected because the zero level of the output of the waveform equalizing circuit (Fig. 10A) represents the data point phase. That is, as shown in Fig. 10A, the interpolation result S^ between the data Xk-1 and Xk is zero in the in-phase condition. However, if the interpolation result S^ is not zero, the value of the interpolation result S^ represents a phase error signal which is outputted by the reproduced bit synchronizing clock generator 62 and supplied to the digital VCO 64 via the digital loop filter 63. The digital VCO 64 generates the bit synchronizing phase signal with the data point phase compensated in accordance with the phase error signal to provide the PLL operation.

[0060] In the above-mentioned embodiments, the prediction data used for the metric operation in the Viterbi decoding is operated in accordance with distribution of sampled values of the equalized waveform to provide optimum values of the prediction data for the metric operation. Moreover, the equalizing error is operated from the equalized waveform and a target equalizing values to adaptively change the frequency characteristic of the waveform equalizing circuit to reduce the equalizing error.

Claims

1. A decoding apparatus for decoding a signal reproduced from an optical disc, the apparatus comprising:

   automatic gain control means for controlling an envelope level of a waveform of said signal to a

predetermined level;

waveform equalizing means having a frequency characteristic for waveform-equalizing said signal from said automatic gain control means to remove reproduction waveform distortion of said signal, said frequency characteristic being changed in accordance with at least a tap coefficient;

binary coding means for binary-coding an output of the waveform equalizing means;

a phase-locked-loop circuit for generating a bit synchronizing clock signal on the basis of an output of said binary coding means;

a/d converting means for a/d-converting an output of said waveform equalizing means in response to said bit synchronizing clock signal;

Viterbi decoding means including metric operation means for Viterbi-decoding said output of the a/d converting means in response to said bit synchronizing clock signal to output a bit stream, said metric operation means generating a metric operation result from an output of the a/d-converting means and prediction data, said Viterbi decoding means Viterbi-decoding said output of said a/d converting means with said metric operation result;

operating means for operating an equalizing error from the output of a/d converting means and waveform equalizing target data;

coefficient generation means for generating said tap coefficient from said equalizing error to minimize the equalizing error; and

means for operating said prediction data in accordance with said output of said a/d converting means.

2. A decoding apparatus for decoding a signal reproduced from an optical disc comprising:

automatic gain control means for controlling an envelope level of a waveform of said signal to a predetermined level;

waveform equalizing means having a frequency characteristic for waveform-equalizing said signal from said automatic gain control means to remove reproduction waveform distortion of said signal, said frequency characteristic being changed in accordance with at least a tap coefficient;

a/d converting means for a/d-converting an output of said waveform equalizing means in response to a sampling clock signal;

bit clock operation and data estimating means responsive to said sampling clock signal for operating a bit synchronizing clock position from an output of said a/d converting means to generate a bit synchronizing clock signal and estimating a level of an output of said a/d converting means at said bit synchronizing clock position to output estimated data;

Viterbi decoding means including metric operation means for Viterbi-decoding said output of said a/d converting means in response to said bit synchronizing clock signal to output a bit stream, said metric operation means generating a metric operation result from an output of said a/d-converting means and prediction data, said Viterbi decoding means Viterbi-decoding said output of said a/d converting means with said metric operation result;

operating means for operating an equalizing error from said output of said a/d converting means and a waveform equalizing target value;

coefficient generation means for generating said tap coefficient from said equalizing error to minimize the equalizing error; and

means for operating said prediction data in accordance with said output of said a/d converting means.

FIG. 1

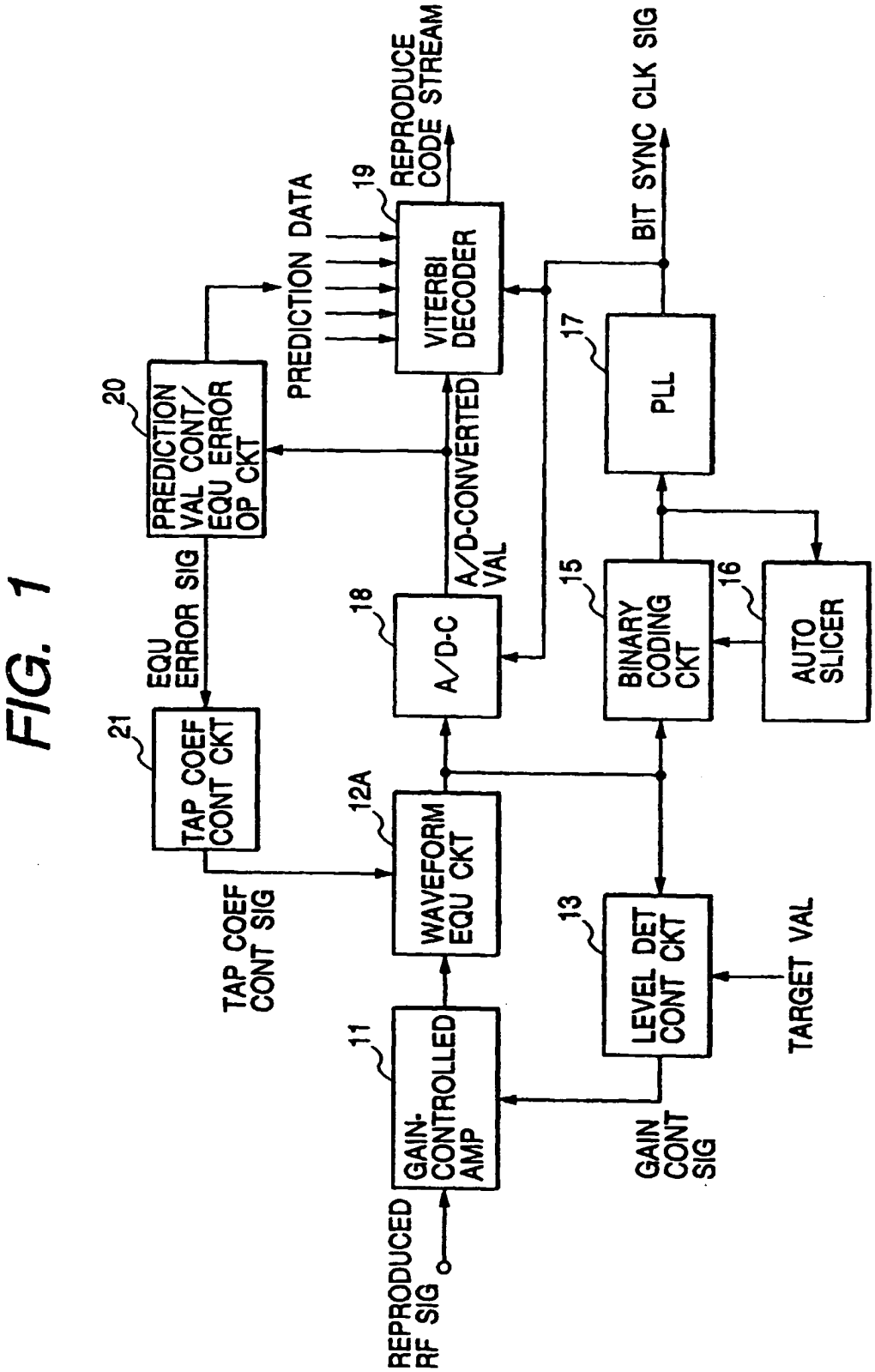
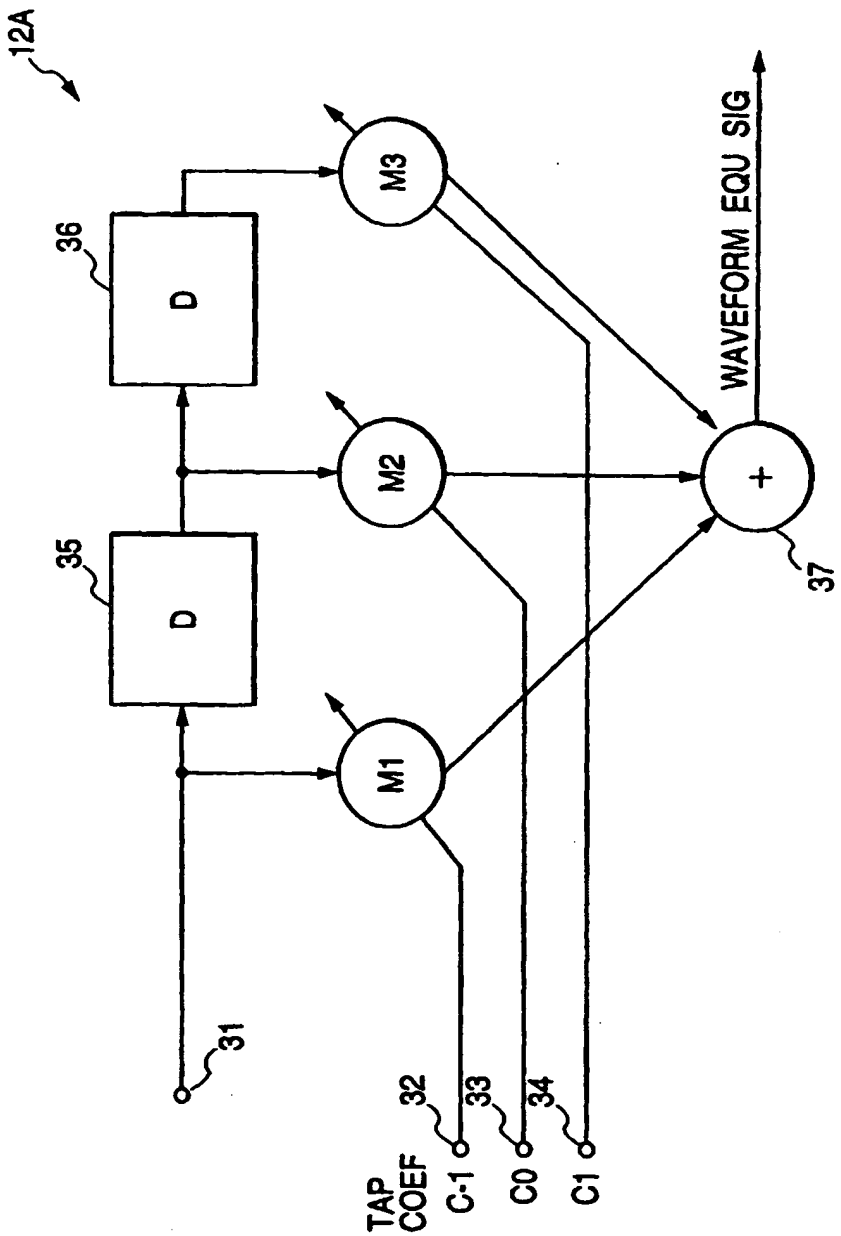

REPRODUCED RF SIG
GAIN-CONTROLLED AMP
11
WAVEFORM EQU CKT
12A
LEVEL DET CONT CKT
13
TARGET VAL
GAIN CONT SIG
TAP COEF CONT SIG
TAP COEF CONT CKT
21
EQU ERROR SIG
PREDICTION VAL CONT/ EQU ERROR OP CKT
20
PREDICTION DATA
A/D-C
18
A/D-CONVERTED VAL
VITERBI DECODER
19
REPRODUCE CODE STREAM
BINARY CODING CKT
15
AUTO SLICER
16
PLL
17
BIT SYNC CLK SIG

FIG. 2


12A
M3
M2
M1
D
D
36
35
31
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33
34
37
+
WAVEFORM EQU SIG
TAP COEF
C-1
C0
C1

FIG. 3A
PRIOR ART

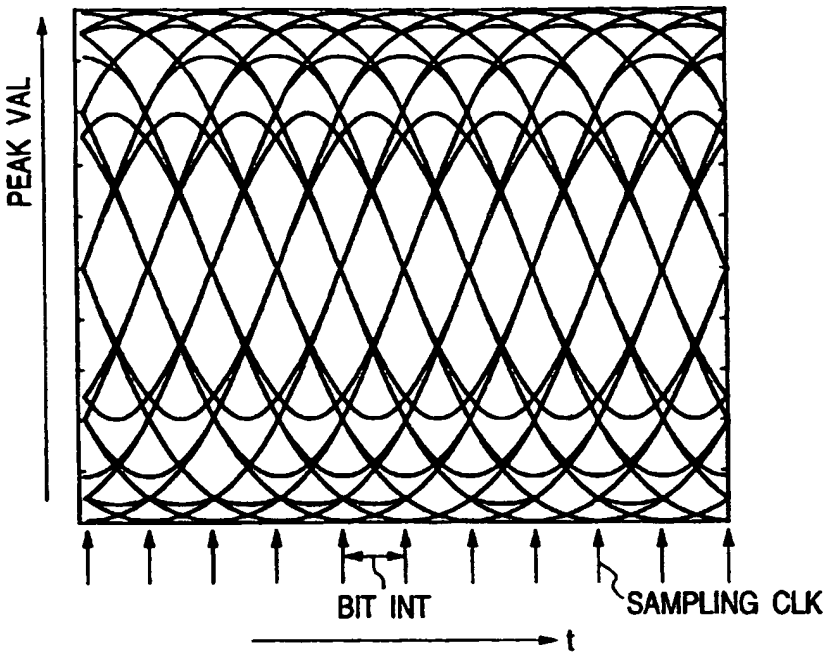


FIG. 3B

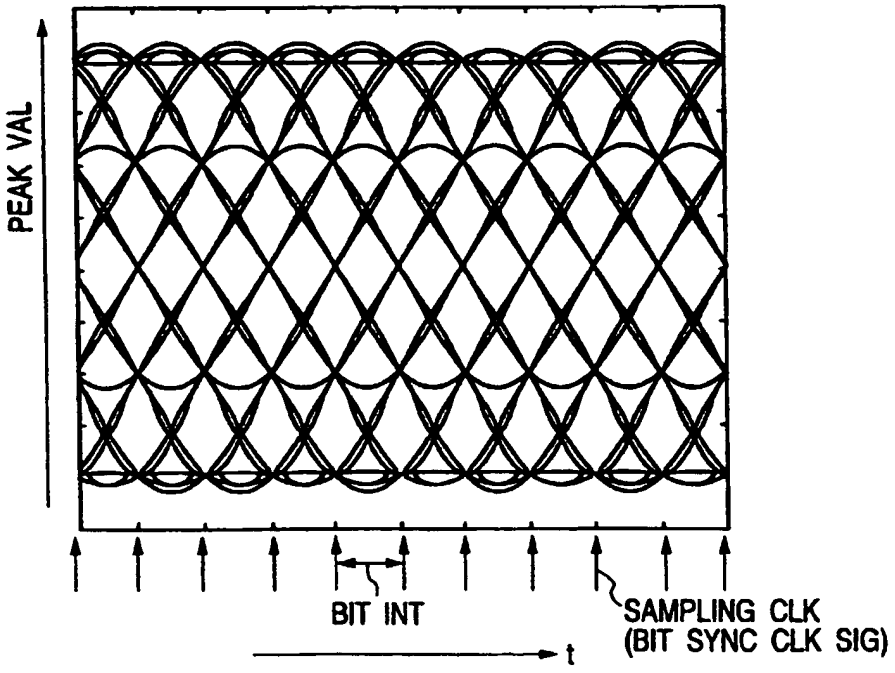


FIG. 4

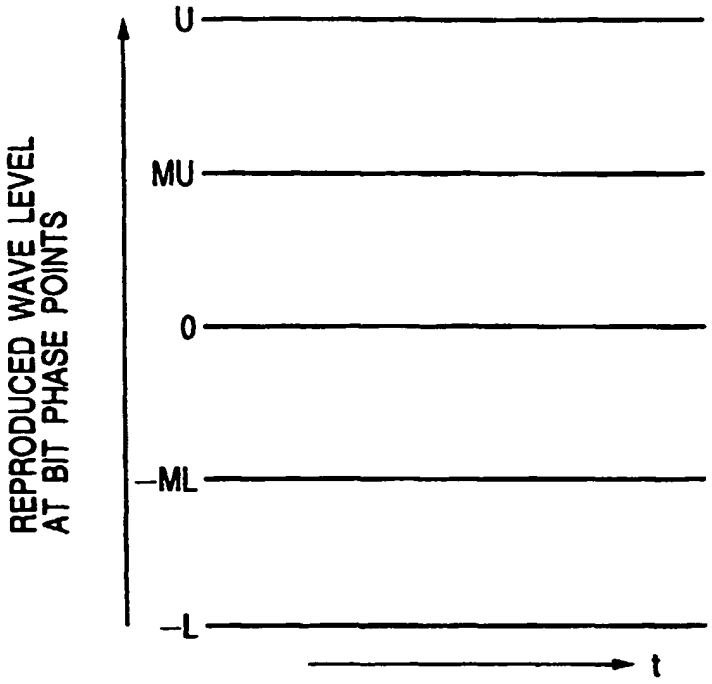


FIG. 5A

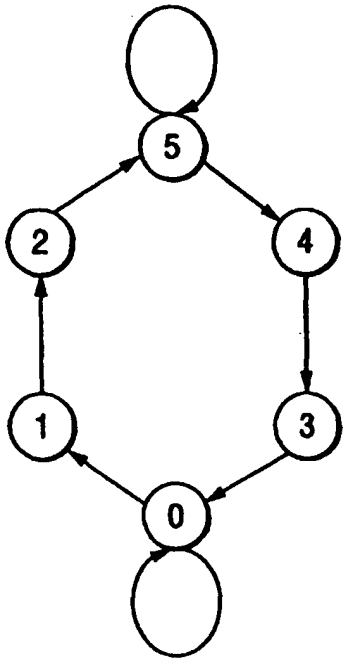


FIG. 5B

COND	DATA VAL
5	111
4	110
3	100
2	011
1	001
0	000

FIG. 6

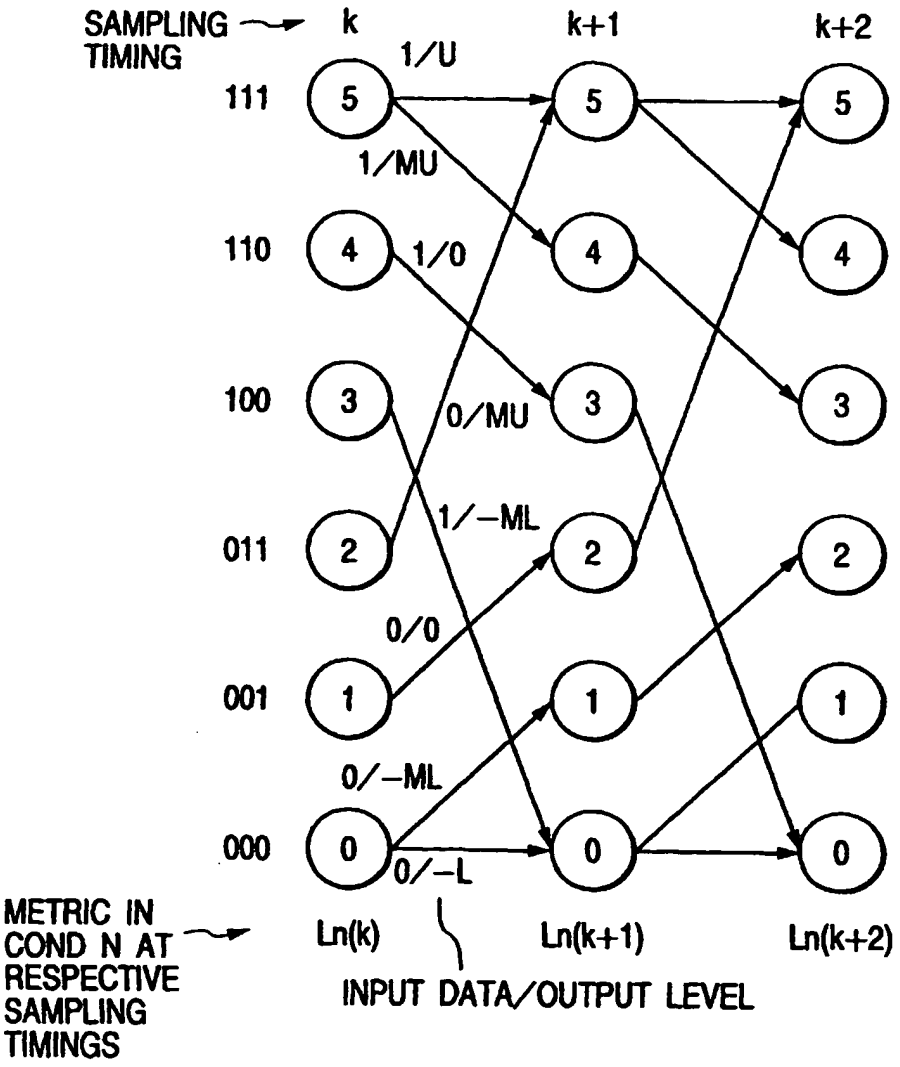

SAMPLING TIMING
k
k+1
k+2
111
110
100
011
001
000
5
4
3
2
1
0
1/U
1/MU
1/0
0/MU
1/−ML
0/0
0/−ML
0/−L
METRIC IN COND N AT RESPECTIVE SAMPLING TIMINGS
Ln(k)
Ln(k+1)
Ln(k+2)
INPUT DATA/OUTPUT LEVEL

FIG. 7

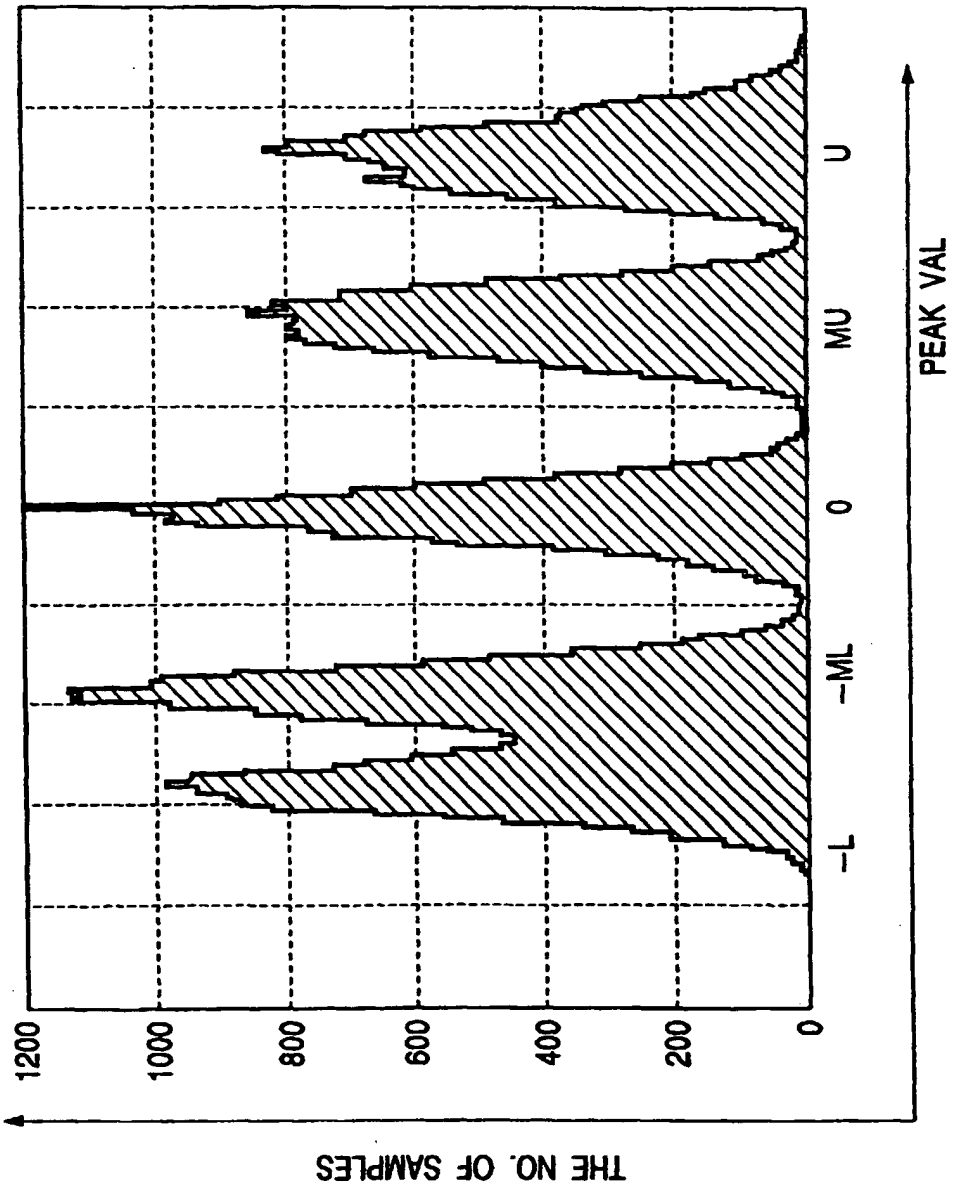


FIG. 8

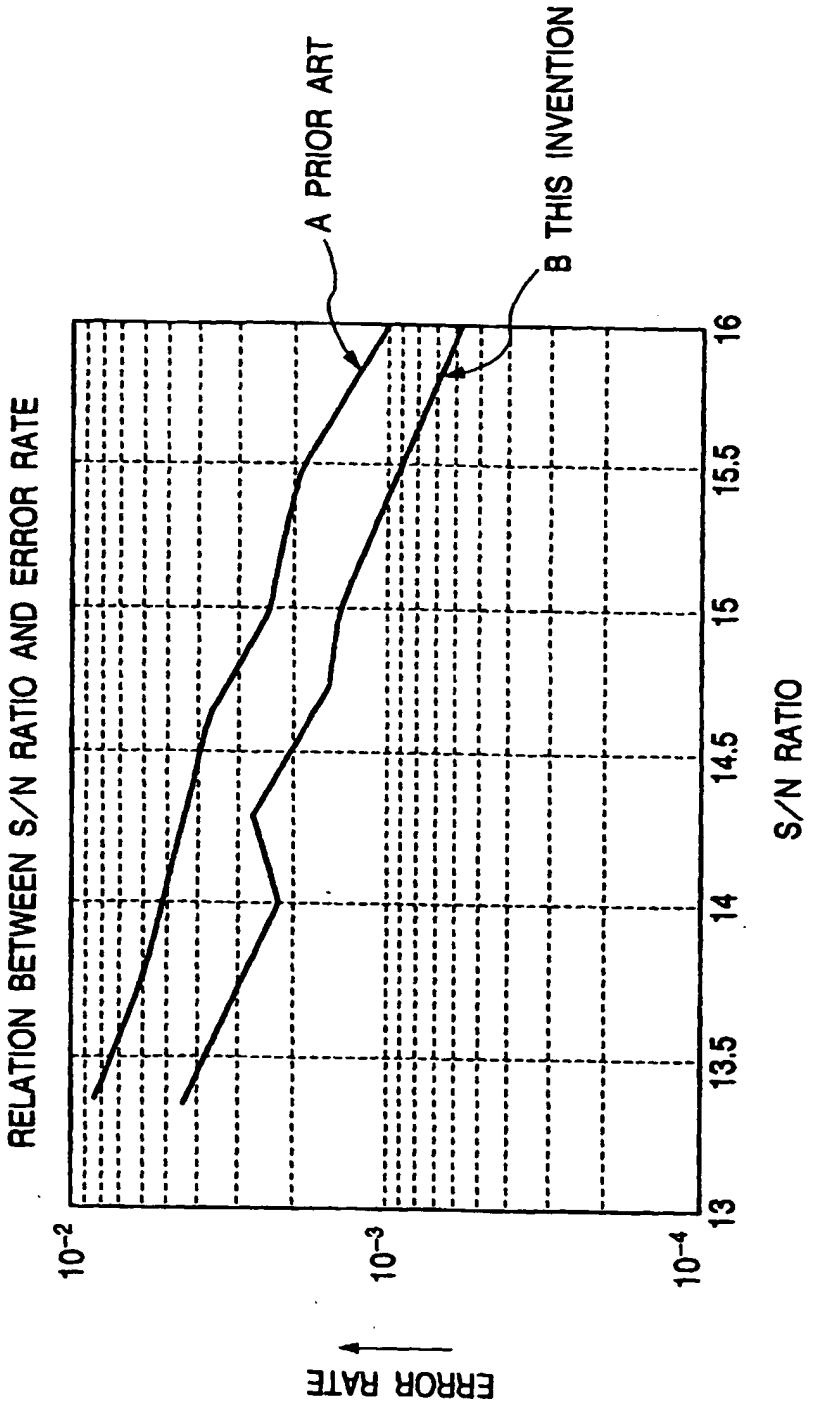
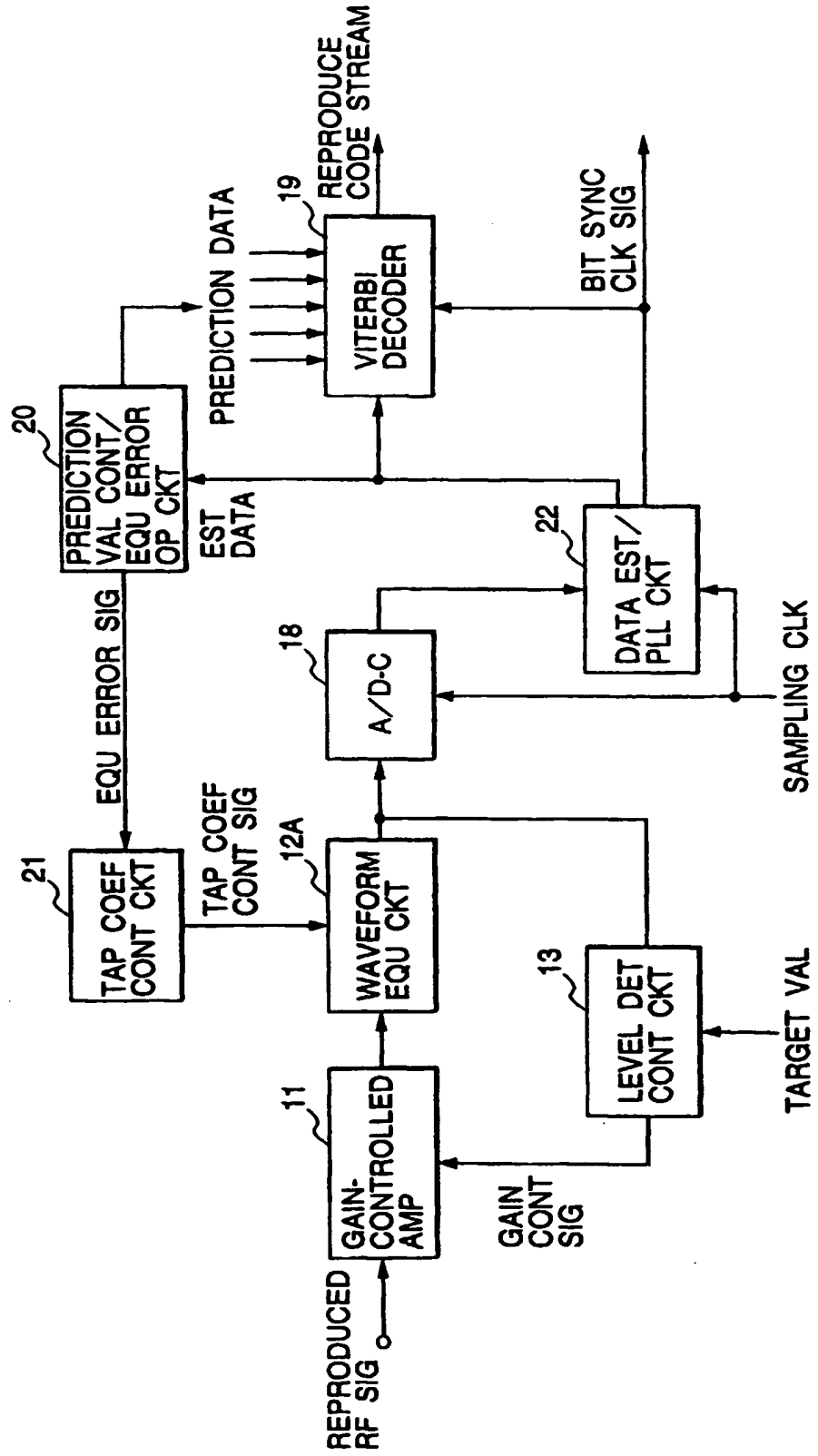

RELATION BETWEEN S/N RATIO AND ERROR RATE
A PRIOR ART
B THIS INVENTION
16
15.5
15
14.5
14
13.5
13
S/N RATIO
10^{-2}
10^{-3}
10^{-4}
ERROR RATE

FIG. 9


REPRODUCED RF SIG
GAIN-CONTROLLED AMP
11
WAVEFORM EQU CKT
12A
A/D-C
18
VITERBI DECODER
19
REPRODUCE CODE STREAM
PREDICTION VAL CONT/ EQU ERROR OP CKT
20
PREDICTION DATA
EST DATA
EQU ERROR SIG
TAP COEF CONT CKT
21
TAP COEF CONT SIG
DATA EST/ PLL CKT
22
LEVEL DET CONT CKT
13
GAIN CONT SIG
BIT SYNC CLK SIG
SAMPLING CLK
TARGET VAL

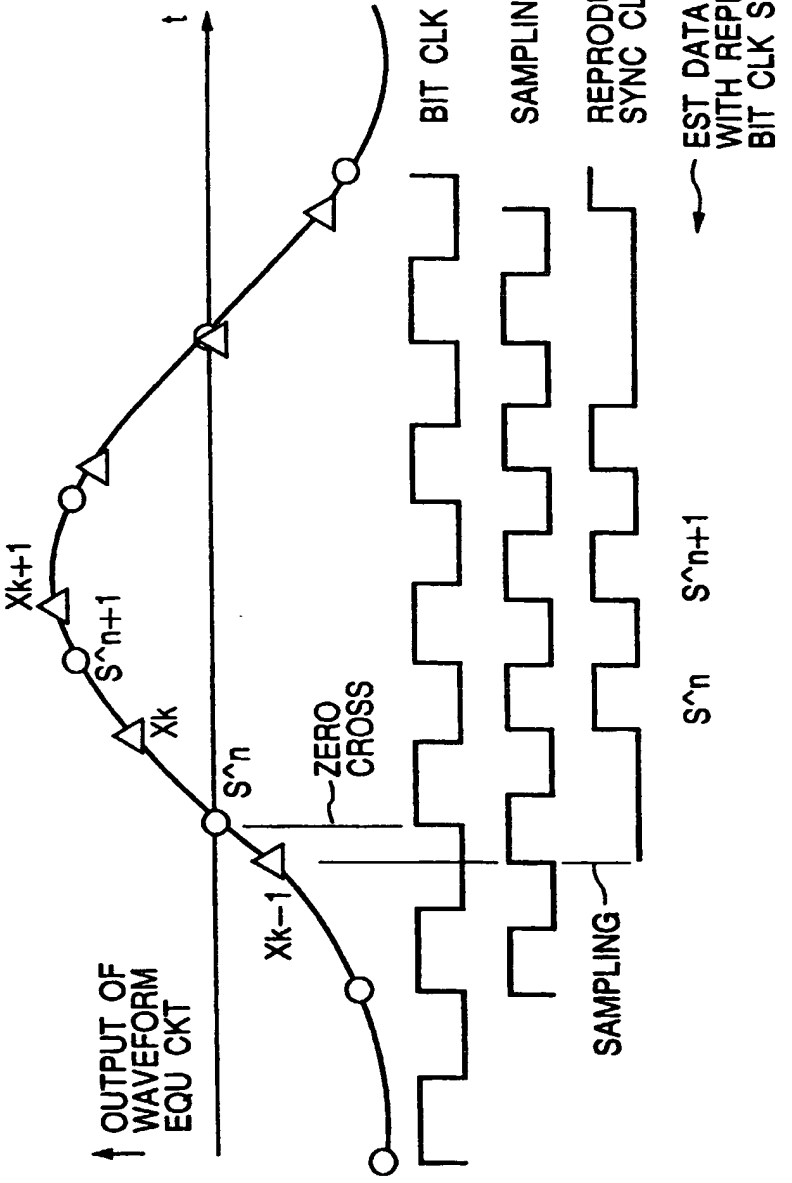


FIG. 10A

FIG. 10B

FIG. 10C

FIG. 10D

FIG. 10E

FIG. 11
PRIOR ART

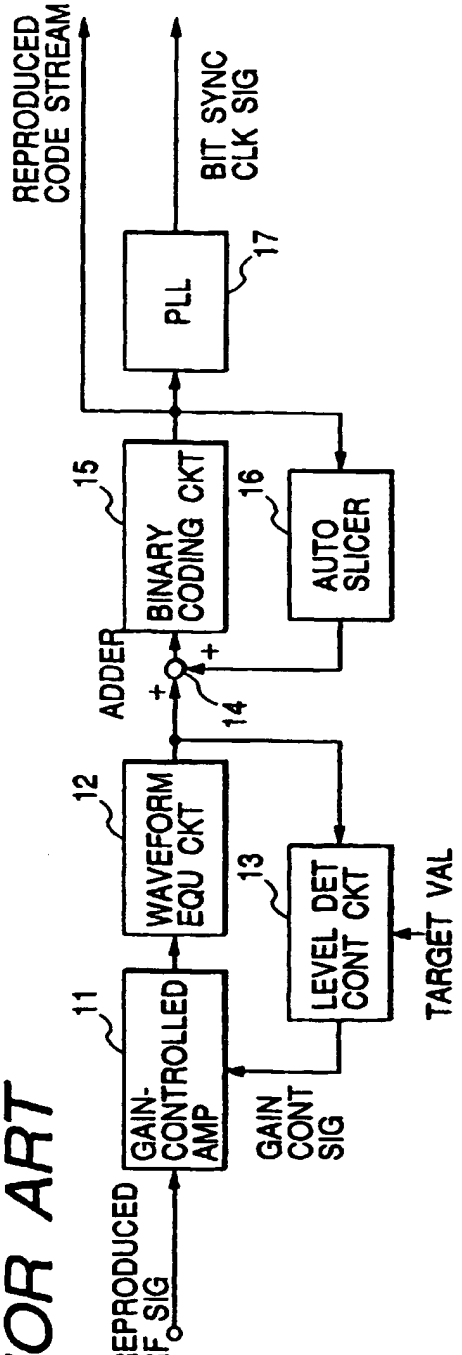


FIG. 12
PRIOR ART

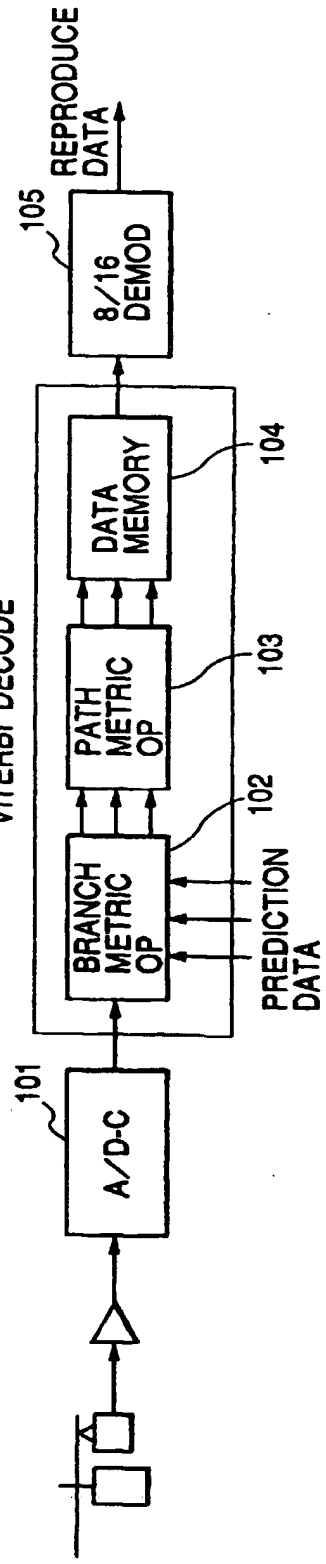


FIG. 13

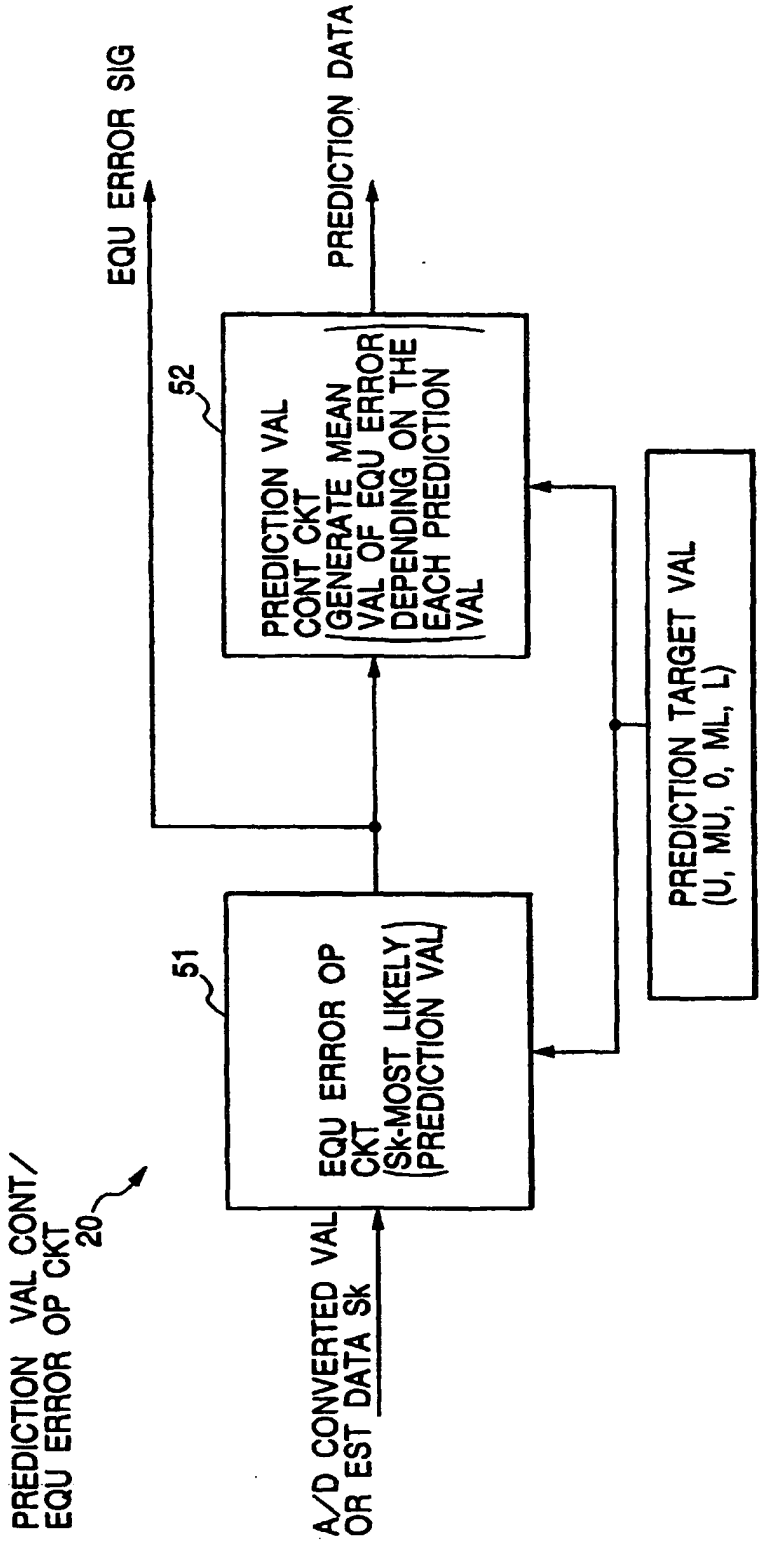
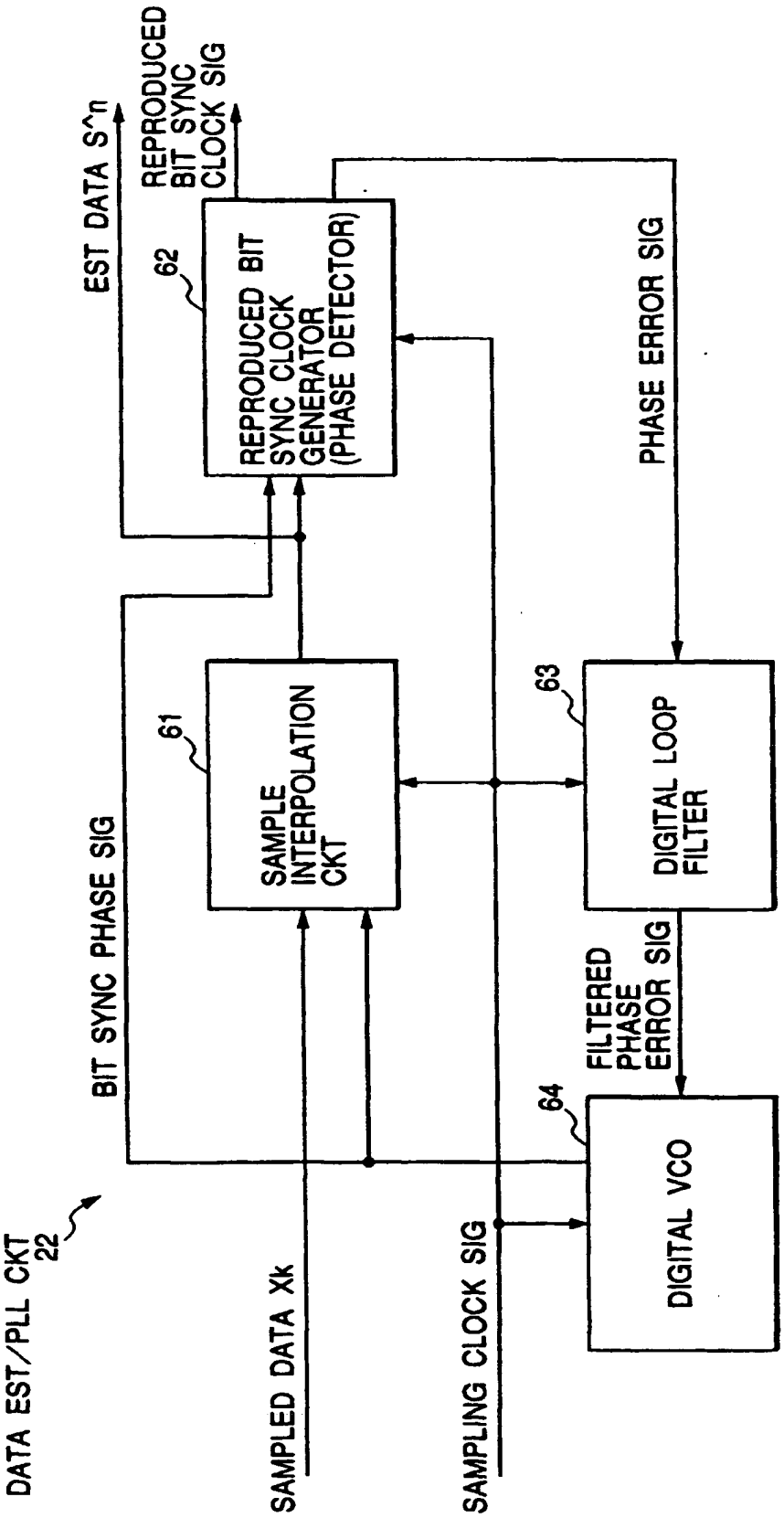

PREDICTION VAL CONT/
EQU ERROR OP CKT
20
A/D CONVERTED VAL
OR EST DATA Sk
51
EQU ERROR OP CKT
(Sk-MOST LIKELY
PREDICTION VAL)
52
PREDICTION VAL
CONT CKT
(GENERATE MEAN
VAL OF EQU ERROR
DEPENDING ON THE
EACH PREDICTION
VAL
PREDICTION TARGET VAL
(U, MU, 0, ML, L)
EQU ERROR SIG
PREDICTION DATA

FIG. 14


DATA EST/PLL CKT
22
BIT SYNC PHASE SIG
EST DATA S^n
REPRODUCED BIT SYNC CLOCK SIG
61
SAMPLE INTERPOLATION CKT
62
REPRODUCED BIT SYNC CLOCK GENERATOR (PHASE DETECTOR)
63
DIGITAL LOOP FILTER
64
DIGITAL VCO
PHASE ERROR SIG
FILTERED PHASE ERROR SIG
SAMPLED DATA Xk
SAMPLING CLOCK SIG

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9596

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 0 652 559 A (FUJITSU LTD) 10 May 1995 (1995-05-10) * figures 9,20 * * page 7, line 53 - page 8, line 21 * * page 15, line 21 - line 48 * ---	1	G11B20/10 H03M13/41 G11B20/14
A	EP 0 751 653 A (MOTOROLA INC) 2 January 1997 (1997-01-02) * figure 1 * * column 1, line 58 - column 2, line 27 * ---	1,2	
A P,A	JP 10 208395 A (CIRRUS LOGIC INC) 7 August 1998 (1998-08-07) & US 5 892 632 A (BEHRENS RICHARD T ET AL) 6 April 1999 (1999-04-06) * column 1, line 24 - line 28 * * column 2, line 23 - line 47 * * column 4, line 48 - line 59 * * column 7, line 19 - column 8, line 3 * * column 8, line 42 - column 9, line 15 * * figure 3 * ---	2 2	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
A	US 5 781 590 A (HONMA HIROMI ET AL) 14 July 1998 (1998-07-14) * column 1, line 7 - line 15 * * column 9, line 58 - column 10, line 24 * * column 19, line 44 - column 20, line 48 * * column 21, line 52 - column 22, line 1 * -----	1,2	G11B H03M H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 March 2000	Ogor, M

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28-03-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0652559 A	10-05-1995	JP 8087828 A	02-04-1996
		US 5986987 A	16-11-1999
		US 5680380 A	21-10-1997
		US 5850377 A	15-12-1998
EP 0751653 A	02-01-1997	US 5590154 A	31-12-1996
		JP 9036782 A	07-02-1997
JP 10208395 A	07-08-1998	US 5892632 A	06-04-1999
US 5781590 A	14-07-1998	JP 2853650 B	03-02-1999
		JP 9288865 A	04-11-1997

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